CONNECTIONS TO CORE ARRAY DRIVE LINES

P25
CM64
MT1 MT2
MT3 MT4

INHIBIT WIRE CONNECTIONS

ROW/COLUMN SELECTION LINES
(FROM ADDRESS DECODER)

SENSE WIRE CONNECTIONS

DATA IN

DATA OUT

CONTROL BIT
RESET
LOAD

64-BYTE FERRITE CORE CARRIER BOARD

Sheet: /	
File: Memory Board.sch	
Title:	
Size: A3	Date: 04/2017 Andrew J. Starr
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